An Integrated Planar Patch-Clamp System

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Abstract: Single ion-channel recording using the conventional patch-clamping technique has several limitations. One of the main challenges is to reduce the background noise associated with the patch-clamp setup. Planar patch-clamping has many advantages, one of which is the reduction of noise by using planar micropipettes built in silicon. In this work, we analyze the various sources of noise present in the patch-clamp system, showing the noise improvements by choosing planar micropipettes. Also, we show the design topology and the fabrication of an integrated planar patch-clamp system.

Introduction to Conventional Patch Clamping with Micropipettes: The study of cellular functions, which is important for fields like pharmacological drug screening, clinical diagnostics and drug discovery, is determined by the opening and closing of 'ion-channels' in the cell membrane [1]. The patch-clamp technique is a method for studying the ion-channel behavior where a small 'patch' of the cell membrane is isolated for localized electrical measurement by placing a glass micropipette onto the surface of a voltage-clamped cell. The electrical model of the cell is shown in Figure 1. A biological cell has ion channels, each type of ion channel being represented by a conductance G_K and a resting potential V_K. The cell membrane contributes a capacitance C_M and the seal formed between the patch and the glass pipette is represented by a conductance G_S. The glass pipette has a resistance R_P and a capacitance C_P associated with it. The electrical parameters of the cell are not constant but may vary during the course of any patch-clamping experiment. Typical values for a 10μm cell are: $G_K = 10^{-9}\Omega^{-1}$, $V_K = 56mV$, $G_S = 1\text{-}2x10^{-11}\Omega^{-1}$, $C_M = 10\text{-}20pF$, $R_P = 10^7\Omega$, $C_P = 0.01pF$.

Motivation for Planar Patch-Clamping: In present-day patch-clamp circuitry, the headstage is a transimpedance amplifier (with a feedback resistor $R_F \sim 50G\Omega$) for whole-cell recording ($I_{WC} \sim 1nA$) while it is a capacitive-feedback integrator for single-channel recording ($I_{SC} \sim 5pA$) [1,2]. In addition to the basic amplifying-filtering circuitry, there are also circuits for series-resistance compensation, high-frequency compensation and capacitive-transients compensation [2,3]. This makes the entire patch-clamp electronics complicated, costly and inappropriate for integration on a chip. One of the main sources of error in patch-clamp experiments is the series resistance R_P associated with the micropipette. Besides the voltage drop across R_P, there is a time constant for charging the cell ($\tau_{cell} \sim R_P.C_M$), which determines how soon the clamp-voltage is applied across the cell. As will be shown later, this pipette resistance R_P (because of the inherent conical shape of the pipette) can be a major source of noise at higher frequencies. Going for planar micropipettes in silicon would reduce this series resistance by orders of magnitude ($R_P' \sim 10\text{-}50k\Omega$), thereby giving improved noise performance. Planar patch-clamping has other advantages of integration-on-a-chip, cost-effectiveness and high-throughput-screening (HTS), which are also worth mentioning.

Noise Analysis and Results: The background noise in single-channel recording determines the maximum bandwidth that will preserve an adequate signal-to-noise ratio. Here we analyze the noise contributions from the different elements in a patch-clamp setup. The real part of the admittance of the pipette-cell electrical model is (Figure 1):

$$Re[Y_T(\omega)] = Re[\,(G_S + G_K + j\omega C_M) / \{1 + (G_S + G_K + j\omega C_M).R_P\} + j\omega C_P\,] \quad (1)$$

An approximated expression ($G_S, G_K << 1$) for Equation (1) is:

$$Y_2(\omega) = \text{approx.}\{Re[Y_T(\omega)]\} = \omega^2 C_M^2 R_P / \{1 + \omega^2 C_M^2 R_P^2\} \quad (2)$$

Figure 2 compares Equation (1) and Equation (2). Decreasing the series resistance R_P (from 10MΩ to 50kΩ) makes the admittance ($Re[Y_T(\omega)]$ or $Y_2(\omega)$) virtually independent of frequency.

Figure 3 shows the various noise sources at the resistive headstage of a patch-clamp setup, with a resistance R_C for the clamp-voltage source V_C. The noise parameters of the low-noise JFET-input opamp (LF155) are $I_N = 10fA/Hz^{1/2}$ and $E_N = 15nV/Hz^{1/2}$ (for f>1kHz).

Using $R_S \equiv 1/Y_2(\omega)$, $E_N^2 = E_{N1}^2 + E_{N2}^2$, $I_N = I_{N1} = I_{N2}$, *the input-noise voltage* is given by:

$$E_{NI}^2 = (1+R_S/R_F)^2.\{E_N^2 + E_{TC}^2 + I_N^2R_C^2\} + E_{TS}^2 + (R_S/R_F)^2.E_{TF}^2 + I_N^2R_S^2 \quad (3)$$

where $E_{TS}^2 = 4kTR_SB$, $E_{TC}^2 = 4kTR_CB$, $E_{TF}^2 = 4kTR_FB$ ('B' being the bandwidth).

The *input-noise current* is given by:

$$I_{NI}^2 = (1/R_S+1/R_F)^2.\{E_N^2 + E_{TC}^2 + I_N^2R_C^2\} + E_{TS}^2 / R_S^2 + E_{TF}^2 / R_F^2 + I_N^2 \quad (4)$$

Figure 4 plots the input-noise voltage from Equation (3). The input-noise current gives a better understanding of the different noises present in the system. Figure 5 and Figure 6 show the input-noise current for various values of R_P with an opamp noise-current of $10fA/Hz^{1/2}$ and $1fA/Hz^{1/2}$ respectively. At frequencies below 700Hz, the total noise-current is dominated by the noise-current of the opamp. But at higher frequencies, it is the noise associated with R_S (or $1/Y_2(\omega)$) that becomes dominant and this impedance is dominated by the pipette resistance R_P (as shown in Figure 2). Figure 7 shows the contribution of the various noise sources in the patch-clamp setup. The noise contributed by the feedback resistance R_F and the clamp-voltage source resistance R_C is less than $1fA/Hz^{1/2}$. For R_P =10MΩ, it is the opamp noise-current (at f <700Hz) and the noise of the pipette resistance (at f>700Hz) which is crucial. Decreasing R_P in the kΩ range leaves the total noise-current mainly dependent on the opamp noise-current.

Figure 8 shows the noise model of a capacitive-feedback headstage with a reset switch across the feedback capacitor C_F. In patch-clamp experiments, as the time duration between resets is long (τ ~10ms), the 'kT/C' of the feedback capacitor C_F can be neglected. Only the leakage current from the reset switch (I_{SW}) adds some uncertainty to the ion-channel current. The *input-noise current* in this case becomes:

$$I_{NI}^2 = (1/R_S)^2.\{E_N^2 + E_{TC}^2 + E_{TS}^2 + I_N^2R_C^2\} + I_N^2 + I_{SW}^2 \quad (5)$$

Figure 9 shows the input-noise current of a patch-clamp system with capacitive-feedback headstage. This figure is quite similar to Figure 5, indicating that the noise contribution from the feedback network is not so important in the total input-referred noise current. But surely, the output-referred noise voltage would be less for the capacitive-feedback as compared to that of resistive-feedback headstage. Decreasing the integration time τ below a certain threshold would make the input-noise current dependent on the kT/C noise of the capacitor C_F also.

Figure 10 shows the topology of the planar patch-clamp structure fabricated in silicon. It consists of a pore (0.5-1μm) in a thin nitride membrane (2000A° thick) resting on an ultra-deep well (325μm deep). Figure 11 shows the silicon wells with the exposed nitride membrane on the other side. Figure 12 shows some pores of various shapes and sizes drilled in the nitride membrane using the Focused-Ion-Beam system. The front and back microelectrodes for probing the ion currents, with the fluid chambers, are fabricated on separate glass substrates and bonded to the silicon substrate. The possibility of making similar structures in silicon with control electrodes acting as the *source* and *drain* of a FET is discussed in the literature [4].

Conclusion: Noise in patch-clamp measurements comes from various sources like the headstage amplifier, the pipette and its holder, the membrane-to-glass seal and the varying electrical parameters of the biological cell. Here, we have studied the noise contributions from different sources in a patch-clamp setup. At low frequencies (f <700Hz), the opamp noise-current is dominant, while at higher frequencies (f >700Hz) the noise due to the pipette resistance becomes crucial. Planar patch-clamping, which uses planar pipettes built in silicon, is a desirable way of approach for noise reduction, integration-on-a-chip and HTS. We have also shown the design topology and fabrication of our planar patch-clamp system.

References:

[1] Bert Sakmann and Erwin Neher, *Single Channel Recording*, Plenum Press, 1995.

[2] Axon Instruments, *Axopatch 200B Manual*, 2000.

[3] F.J. Sigworth, "Design of the EPC-9, a computer-controlled patch-clamp amplifier. 1.Hardware," *Jour. of Neurosci. Methods*, vol. 56, pg.195-202 (1995).

[4] Erwin Neher, "Molecular Biology meets microelectronics," *Nature*, vol. 19, pg.114 (Feb. 2001).

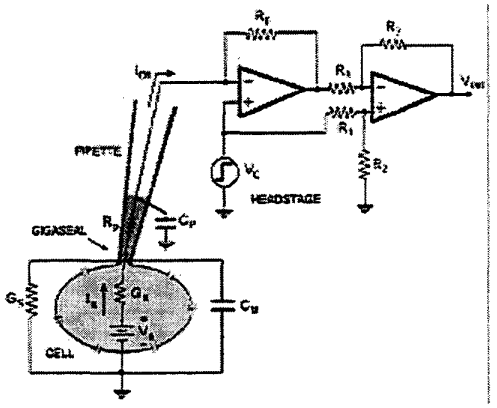

Figure 1: The 'whole-cell' patch-clamp setup showing the electrical model of the cell.

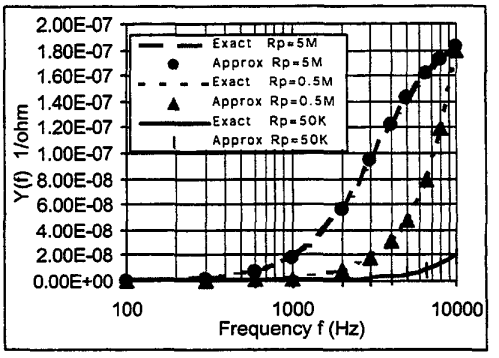

Figure 2: Comparison between the exact admittance and the approximated admittance (Equations (1,2)). (C_M=10pF, G_S=2x10$^{-11}\Omega^{-1}$, G_K=1x10$^{-9}\Omega^{-1}$)

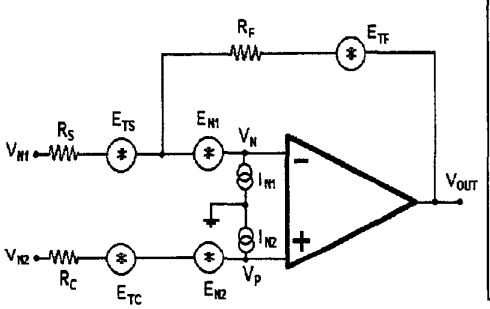

Figure 3: Noise sources at the resistive headstage of a patch-clamp setup.

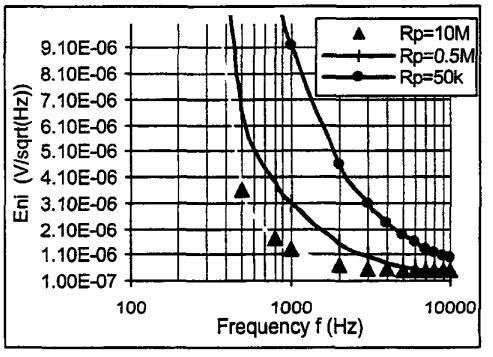

Figure 4: Total input-noise-voltage Eni for Figure 3. (R_C=1kΩ, R_F=10GΩ , B=10kHz, C_M=10pF, $R_S \equiv 1/Y_2(\omega)$, E_N~15nV/Hz$^{1/2}$, I_N=10fA/Hz$^{1/2}$)

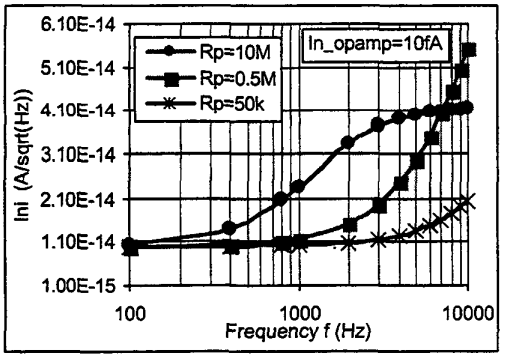

Figure 5: Total input-noise-current Ini for Figure 3. (R_C=1kΩ, R_F=10GΩ , B=10kHz, C_M=10pF, $R_S \equiv 1/Y_2(\omega)$, E_N~15nV/Hz$^{1/2}$, I_N=10fA/Hz$^{1/2}$)

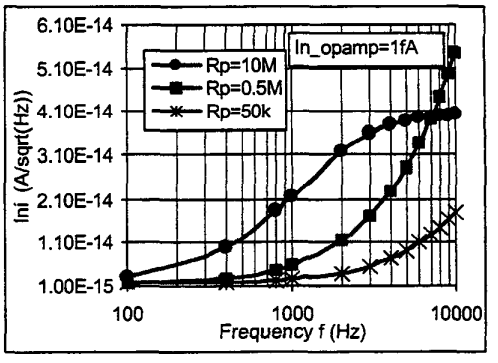

Figure 6: Total input-noise-voltage Ini for Figure 3. (R_C=1kΩ, R_F=10GΩ , B=10kHz, C_M=10pF, $R_S \equiv 1/Y_2(\omega)$, E_N~15nV/Hz$^{1/2}$, I_N=1fA/Hz$^{1/2}$)

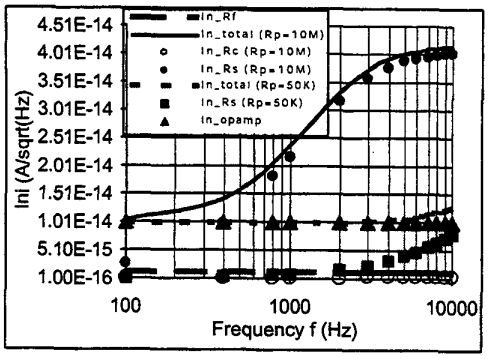

Figure 7: Noise-current contributions for Figure 3. (R_C=1kΩ, R_F=10GΩ , B=10kHz, C_M=10pF, R_S≡1/$Y_2(\omega)$, E_N~15nV/$Hz^{1/2}$, I_N=10fA/$Hz^{1/2}$)

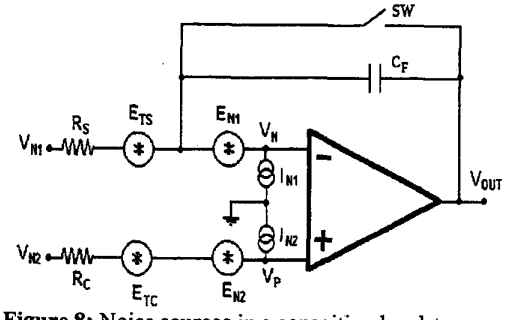

Figure 8: Noise sources in a capacitive-headstage patch-clamp setup with a reset switch across C_F.

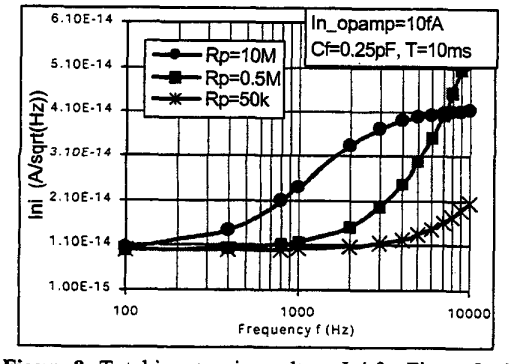

Figure 9: Total input-noise-voltage Ini for Figure 8. (R_C=1kΩ, C_F=0.25pF , B=10kHz, Isw=0.1pA, C_M=10pF, R_S≡1/$Y_2(\omega)$, E_N~15nV/$Hz^{1/2}$, I_N=10fA/$Hz^{1/2}$)

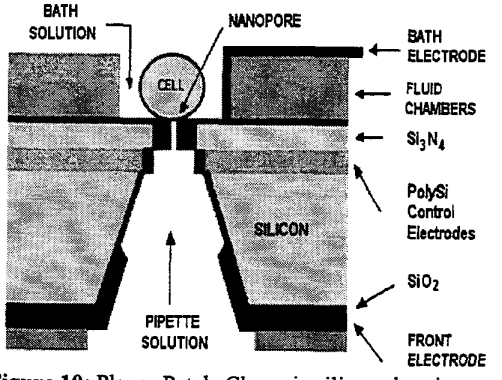

Figure 10: Planar Patch-Clamp in silicon showing the topology of the setup.

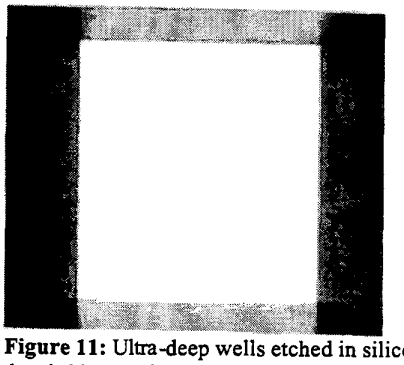

Figure 11: Ultra-deep wells etched in silicon with the nitride membrane on the other side.

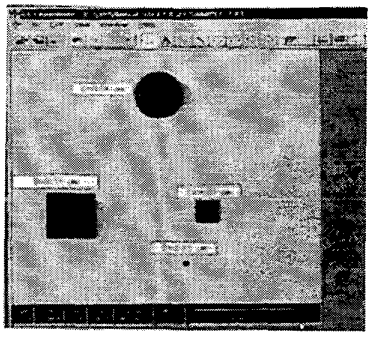

Figure 12: Pores of various shapes and sizes drilled in the nitride membrane using FIB.